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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/696,525	10/29/2003	Chieng-Chung Chen	500-004	6390

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EXAMINER	
PHAN, TRONG Q	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 12/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/696,525	CHEN, CHIENG-CHUNG	
	Examiner	Art Unit	
	TRONG PHAN	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 October 2006*.

2a)☒ This action is **FINAL**. 2b☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,7-9,12 and 13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-9 and 11-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 8 is objected to because of being dependent on cancelled claim 6.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 7, 9 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Fig. 1 Prior Art, in view of Liu, 5,796,670, and Countryman, Jr., 4,532,611.

Regarding claims 1, 7, 9 and 12:

Applicant's Fig. 1 Prior Art discloses a memory pumping circuit comprising:

charging capacitor 12 (see lines 15-17, page 1 of the original specification);

current source 11;

node located between current source 11 and charging capacitor 12 for providing a pumping voltage VPP used as a voltage source for a word line;

driving inverter circuit 13, receiving input clock signal 01, for generating clock signal 02 to drive charging capacitor 12.

Applicant's Fig. 1 Prior Art discloses everything except a DRAM cell as recited in claims 1 and 9.

Liu, 5,796,670, discloses in Fig. 3 a DRAM cell 30 comprising:

select transistor 12;

DRAM cell capacitor, comprising storage capacitor 22 connected in series with storage capacitor 32, including a floating polysilicon, which temporarily retains a charge of electrons indicative of access data for the DRAM device (see lines 19-21, 37-39, column 6; line1-7, column 7).

It would have been obvious under 35 USC 103(a) to one of ordinary skill in the art at the time of the invention was made to utilize the DRAM cell capacitor 22/32 in Fig. 3 of Liu, 5,796,670, for the charging capacitor 12 in Applicant' s Fig. 1 Prior Art for the purpose of providing high data storage capacity and low power consumption (see lines 29-32, column 1 of Liu, 5,796,670).

Applicant's Fig. 1 Prior Art, which is modified by Liu, 5,796,670, disclose everything a DRAM cell comprising a MOS transistor and a storage capacitor as recited in claims 1 and 9.

Countryman, Jr., 4,532,611, discloses in Fig. 5 a fuse link circuit for use in memory device including MOS charging capacitor 37 having source, drain and gate connected together by diode-connected MOS transistor 38 and floating gate 41; wherein: without transistors 36 and 39, the gate voltage Vpp is coupled to the source and the drain of MOS transistor 37 without any voltage drop regardless of the presence of diode-connected MOS transistor 38 (see lines 5-16, column 5).

It would have been obvious under 35 USC 103(a) to one of ordinary skill in the art at the time of the invention was made to utilize the MOS charging capacitor 37 in

Fig. 5 of Countryman, Jr., 4,532,611, for the charging capacitor 32 in Applicant' s Fig. 1 Prior Art, which is modified by Liu, 5,796,670, for the purpose of providing a relative large capacitance (see lines 20-21, column 5 of Countryman, Jr., 4,532,611).

4. Claims 8 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Fig. 1 Prior Art, in view of Liu, 5,796,670, and Countryman, Jr., 4,532,611, and further in view of Hiratsuka et al., 5,453,707.

Applicant's Fig. 1 Prior Art, which is modified Liu, 5,796,670, and Countryman, Jr., 4,532,611, discloses everything except the driving circuit comprising a PMOS transistor and a NMOS transistor for generating a clock signal according to a first clock signal and a second clock signal as recited in claims 8 and 13.

Hiratsuka et al., 5,453,707, discloses in Fig. 4 the teaching of using CMOS inverter 18 consists of PMOS transistor Mp1 and NMOS transistor Mn1 to generate first clock signal 01 according to second clock signal at the output of NAND gate 12 and third clock signal at the output of NOR gate 13 having different phases with each other as shown in Fig. 5.

It would have been obvious under 35 USC 103(a) to one of ordinary skill in the art at the time of the invention was made to utilize the CMOS inverter 18 in Figs. 4-5 of Hiratsuka et al., 5,453,707, for the driving inverter circuit 13 in Applicant's Fig. 1 Prior Art, which is modified by Liu, 5,796,670, and Countryman, Jr., 4,532,611, for the purpose of reducing power dissipation and preventing power source noise and ground noise (see lines 43-49, column 3 of Hiratsuka et al., 5,453,707).

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Response to Arguments

6. Applicant's arguments filed on 10/18/06 have been fully considered and are persuasive. Therefore, the last office action of 7/20/06 has been withdrawn.

However, in view of Applicant's amendments to the claims, a new office action has been set forth and made FINAL as above.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to TRONG PHAN whose telephone number is (571) 272-1794. The examiner can normally be reached on M-F (8:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, AMIR ZARABIAN can be reached on (571)272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Phan Trong

TRONG PHAN
PRIMARY EXAMINER